National Semiconductor

MICROCIRCUIT DATA SHEET

MNLF157-X REV 1A1

Original Creation Date: 06/20/95
Last Update Date: 09/12/02
Last Major Revision Date: 09/05/02

MONOLITHIC JFET INPUT OPERATIONAL AMPLIFIERS

General Description

These are the first monolithic JFET input operational amplifiers to incorporate well matched, high voltage JFETs on the same chip with standard bipolar transistors (BI-FET(TM) Technology). These amplifiers feature low input bias and offset currents/low offset voltage and offset voltage drift, coupled with offset adjust which does not degrade drift or common-mode rejection. The devices are also designed for high slew rate, wide bandwidth, extremely fast settling time, low voltage and current noise and a low 1/f noise corner.

Industry Part Number

LF157

NS Part Numbers

LF157H/883

Prime Die

LF157

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (°C)
	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- Low input bias current	30 pA
- Low input offset current	3 pA
- High input impedance	10e12 Ohms
- Low input offset voltage	1 mV
- Low input offset voltage temp. drift	3 uV/ C
- Low input noise current	0.01 pA/sqrtHz
- High common-mode rejection ratio	100 dB
- Large dc voltage gain	106 dB
- Extremely fast settling time to 0.01%	1.5 uS
- Fast slew rate	50 V/uS
- Wide gain bandwidth	20 MHz
- Low input noise voltage	12 nV/sqrtHz

(Absolute Maximum Ratings)
(Note 1)

Supply Voltage	±22V
Differential Input Voltage	±40V
Input Voltage Range (Note 4)	±20V
Output Short Circuit Duration	Continuous
Tjmax	150 C
Power Dissipation at Ta=25 C (Still Air) (Note 2, 3)	560mW
(500 LF/Min Air Flow)	1200mW
Thermal Resistance ThetaJA (Still Air)	162 C/W
(500LF/Min Air flow)	89 C/W
ThetaJC	32 C/W
Storage Temperature Range	-65 C ≤ Ta ≤ +150 C
Lead Temperature (Soldering, 10 seconds)	300 C
ESD tolerance (Note 5)	1200V

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by Tjmax (maximum junction temperature), ThetaJA (package junction to ambient thermal resistance), and TA (ambient temperature). The maximum allowable power dissipation at any temperature is Pdmax = (Tjmax - TA)/ThetaJA or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 3: Maximum Power Dissipation is deined by the package characteristics. Operating the part near the Maximum Power Dissipation may cause the part to operate outside guaranteed limits.

Note 4: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 5: Human body model, 100pF discharged through 1.5k Ohms.

Electrical Characteristics

DC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vcc = ±15V, Vcm = 0V, Rs = 50 Ohms

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vio	Input Offset Voltage				-5	5	mV	1
					-7	7	mV	2, 3
		Vcc = ±20V			-5	5	mV	1
					-7	7	mV	2, 3
Iio	Input Offset Current				-0.02	0.02	nA	1
					-20	20	nA	2, 3
		Vcm = 11V			-0.02	0.02	nA	1
					-20	20	nA	2, 3
		Vcm = -11V			-0.02	0.02	nA	1
					-20	20	nA	2, 3
		Vcc = ±20V			-0.02	0.02	nA	1
					-20	20	nA	2, 3
Ibias	Input Bias Current					0.1	nA	1
						50	nA	2, 3
		Vcm = 11V				0.1	nA	1
						50	nA	2, 3
		Vcm = -11V				0.1	nA	1
						50	nA	2, 3
		Vcc = ±20V				0.1	nA	1
						50	nA	2, 3
PSRR	Power Supply Rejection Ratio	Vcc = ±20V to ±10V			85		dB	1, 2, 3
CMRR	Common Mode Rejection Ratio	Vcm = ±11V			85		dB	1, 2, 3
+Vio/Adj	Input Offset Voltage Adjust				10		mV	1, 2, 3
-Vio/Adj	Input Offset Voltage Adjust					-10	mV	1, 2, 3
Icc	Power Supply Current					7	mA	1
						9	mA	2, 3
		Vcc = ±20V				9	mA	1
+Ios	Short Circuit Current	Vout = 0V			-35	-15	mA	1

Electrical Characteristics

DC PARAMETERS(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vcc = ±15V, Vcm = 0V, Rs = 50 Ohms

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
-Ios	Short Circuit Current	Vout = 0V			15	35	mA	1
+Vop	Output Voltage Swing	Rl 10K Ohms			12		V	4, 5, 6
		Rl 2K Ohms			10		V	4, 5, 6
-Vop	Output Voltage Swing	Rl 10K Ohms				-12	V	4, 5, 6
		Rl 2K Ohms				-10	v	4, 5, 6
+Avs	Large Signal Voltage Gain	Rl = 2K Ohms, Vout = 0 to 10V			50		V/mV	4
					25		V/mV	5, 6
-Avs	Large Signal Voltage Gain	Rl = 2K Ohms, Vout = 0 to -10V			50		V/mV	4
					25		V/mV	5, 6

AC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Vcc = ±15V, Vcm = 0V, Rs = 50 Ohms

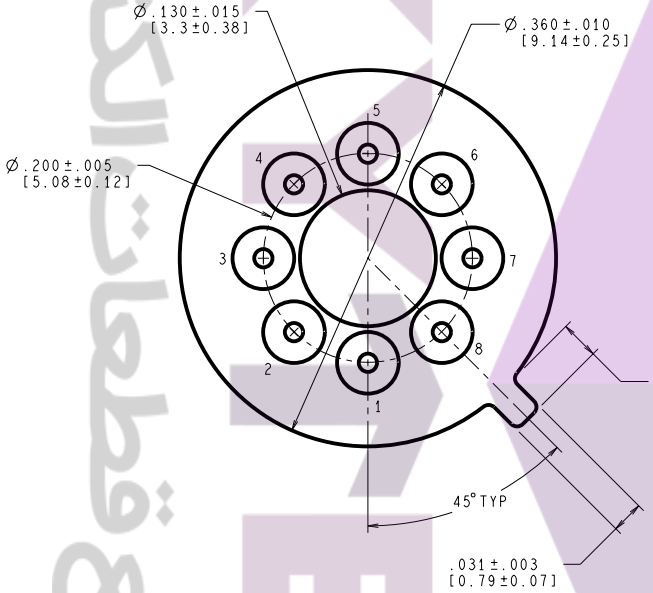
+Sr	Slew Rate	Av = 5, Rload = 2K Ohms, Cload = 100pfd, Vin = -1V to +1V, Vout = -5V to +5V			30		V/uS	9
-Sr	Slew Rate	Av = 5, Rload = 2K Ohms, Cload = 100pfd, Vin = +1V to -1V, Vout = +5V to -5V			30		V/uS	9
Gbw	Gain Bandwidth				15		MHz	9

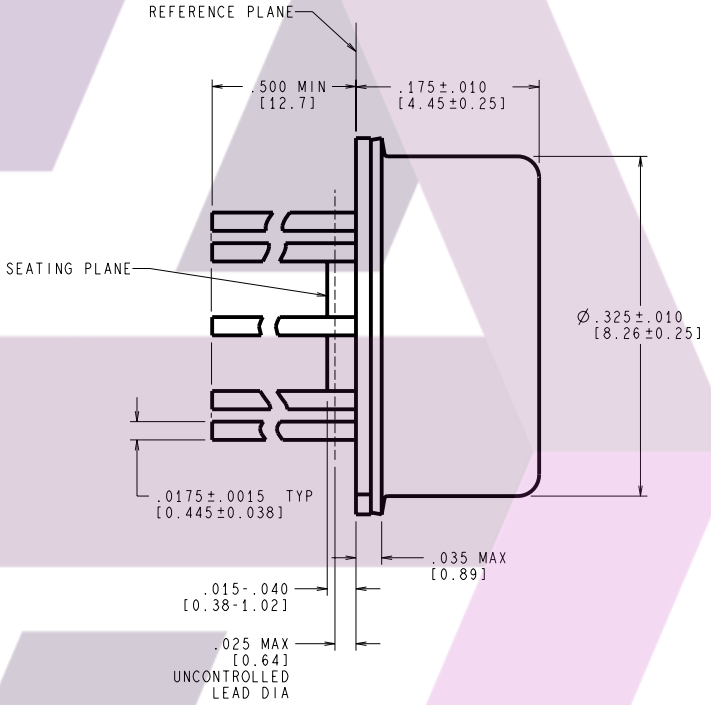
Graphics and Diagrams

GRAPHICS#	DESCRIPTION
05094HRB3	METAL CAN (H), TO-99, 8LD .200 DIA P.C. (B/I CKT)
H08CRF	METAL CAN (H), TO-99, 8LD, .200 DIA P.C. (P/P DWG)
P000295A	METAL CAN (H), 8 LEAD (PINOUT)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
F	REVISE & REDRAW PER CURRENT STANDARD; UPDATE MIL/AERO STAMP & TITLE.	11002	06/22/95	MS/





CONTROLLING DIMENSION IS INCH
VALUES IN [] ARE MILLIMETERS

MIL-I-38535
CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEADS TO BE LOCATED WITHIN .007 IN/ 0.18 mm OF THEIR TRUE POSITIONS RELATIVE TO A MAXIMUM WIDTH TAB.
2. STANDARD METAL CAN TYPE: SOLID BASE WITH CERAMIC STANDOFF.
3. APPLIES TO MIL-AERO AND LINEAR PRODUCTS.
4. REFERENCE JEDEC REGISTRATION TO-99, JEDEC PUBLICATION No.95.

APPROVALS	DATE
DRAWN: MARTA SUCHY	06/22/95
DFTG. CHK.	
ENGR. CHK.	

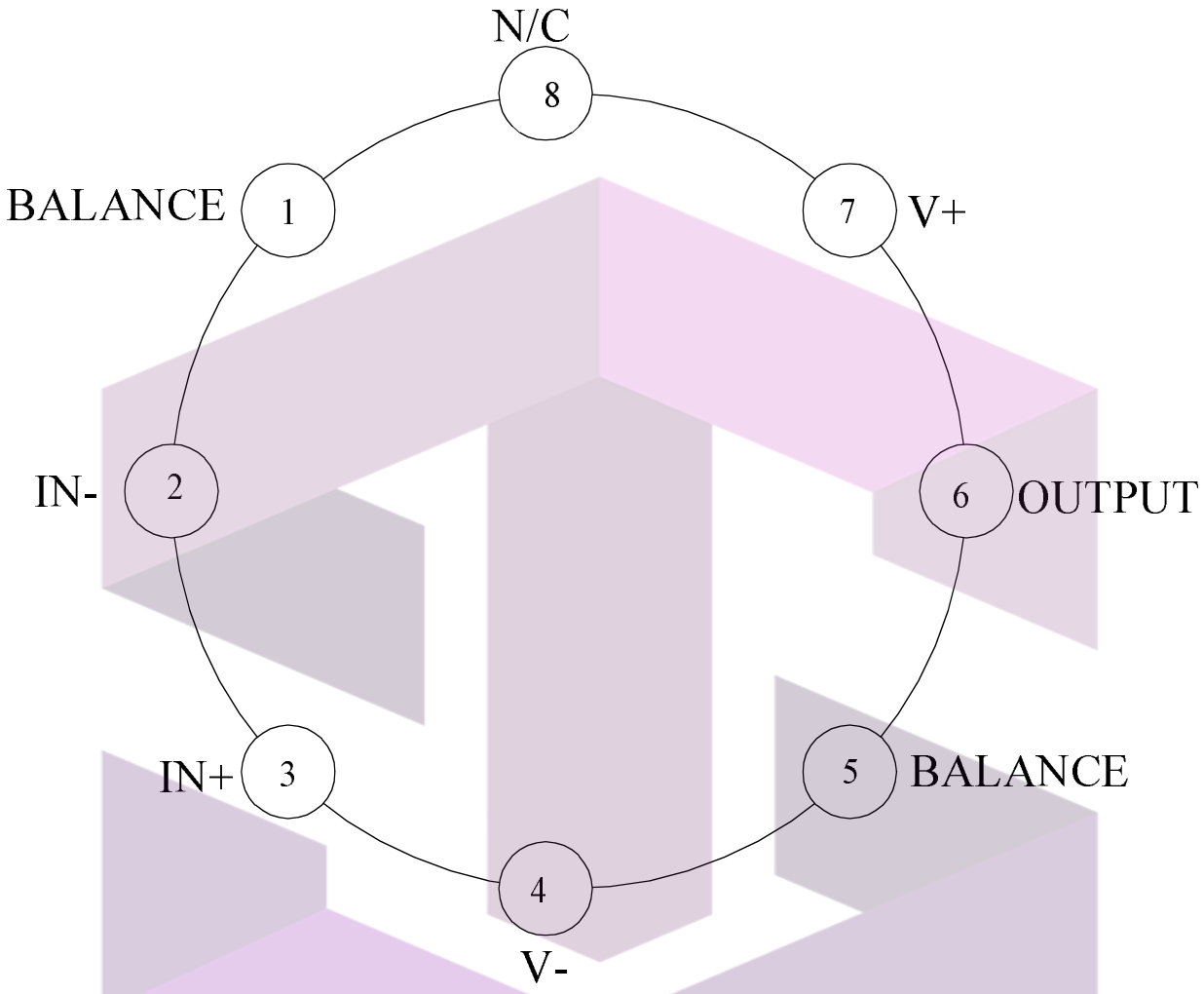
National Semiconductor
2900 Semiconductor dr, Santa Clara, CA 95052-8090

METAL CAN, TO-99, 8 LEAD, .200 DIA P.C.

PROJECTION — INCH [MM]

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-H08C	F

DO NOT SCALE DRAWING | SHEET 1 of 1



LF157AH, LF157H
8 - PIN METAL CAN
CONNECTION DIAGRAM
TOP VIEW
P000295A

National Semiconductor
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050

Revision History

Rev	ECN #	Rel Date	Originator	Changes
1A1	M0004064	09/12/02	Rose Malone	Update MDS to fully Released datasheet: MNLF157-X, Rev. 0BL to MNLF157-X, Rev. 1A1. Changed AC Parameters Section, +SR Condition From: Av = 5, Vin = -5V to +5V TO: Av = 5, Rload = 2K Ohms, Cload = 100pfd, Vin = -1V to +1V, Vout = -5V to +5V and -SR Condition From: Av = 5, Vin = +5V to -5V TO: Av = 5, Rload = 2K Ohms, Cload = 100pfd, Vin = +1V to -1V, Vout = +5V to -5V . Condition Changed to match Test Tape.